MULTIPLE DATA RATES IN PROGRAMMABLE
LOGIC DEVICE SERIAL INTERFACE

Abstract of the Disclosure

[0039] A serial interface for a programmable logic device supports a higher physical medium attachment ("PMA") data rate than the available physical coding sublayer ("PCS") data rate by using multiple PCS modules, operating in parallel, to support one PMA module. In a channel-based structure, the PMA module is supported by a PCS module in its own channel and at least one PCS module from a second channel. The second channel may include its own PMA module which, if provided, may operate at a lower rate, supportable by the PCS module in that channel. Optionally, two modes are provided. In one mode, two PCS modules in two channels support one higher-speed PMA module in one of the channels. In a second mode, each PCS module supports a PMA module in its own channel, with the higher-speed PMA module constrained to operate at the lower data rate of the PCS module.